



PTO/SB/08A (08-03)

Substitute for form 1449A/PTO		<b>Complete if Known</b>	
		Application Number	10/645,788
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Filing Date	August 20, 2003
		First Named Inventor	Maangat, Simar
		Art Unit	2855
		Examiner Name	To Be Assigned
		Attorney Docket Number	015114-067800US
Sheet	1	of	3

U.S. PATENT DOCUMENTS+					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <sup>2</sup> (if known)			
ml	0001	US-4,719,369	01-12-1988	Asano et al.	
	0002	US-4,954,729	09-04-1990	Ural	
	0003	US-5,111,081	05-05-1992	Atallah	
	0004	US-5,134,311	07-28-1992	Biber et al.	
	0005	US-5,184,663	11-17-1992	Alcom	
	0006	US-5,179,300	01-12-1993	Rolandi et al.	
	0007	US-5,359,235	10-25-1994	Coyle et al.	
	0008	US-5,374,861	12-20-1994	Kubista	
	0009	US-5,592,510	01-07-1997	Van Brunt et al.	
	0010	US-5,602,494	02-11-1997	Sundstrom	
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	0018	US-6,008,665	12-28-1999	Kalb et al.	
	0019	US-6,026,456	02-15-2000	Ilkbahar	
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	0022	US-6,064,224	05-16-2000	Esch, Jr. et al.	
	0023	US-6,087,847	07-11-2000	Mooney et al.	
	0024	US-6,097,208	08-01-2000	Okajima et al.	
	0025	US-6,100,713	08-08-2000	Kalb et al.	
	0026	US-6,118,310	09-12-2000	Esch, Jr.	
	0027	US-6,147,520	11-14-2000	Kothandaraman et al.	
	0028	US-6,154,060	11-28-2000	Morriss	
	0029	US-6,157,206	12-05-2000	Taylor et al.	
	0030	US-6,181,157 B1	01-30-2001	Fiedler	
	0031	US-6,236,231 B1	05-22-2001	Nguyen	
	0032	US-6,252,419 B1	08-28-2001	Sung et al.	
	0033	US-6,329,836 B1	12-11-2001	Drost et al.	

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u	0034	US-6,356,106 B1	03-12-2002	Greeff et al.	
	0035	US-6,362,644 B1	03-26-2002	Jeffrey et al.	
	0036	US-6,366,128 B1	04-02-2002	Ghia et al.	
	0037	US-6,411,126 B1	06-25-2002	Tinsley et al.	
	0038	US-6,414,512 B1	07-02-2002	Moyer	
	0039	US-6,424,169 B1	07-23-2002	Partow et al.	
	0040	US-6,433,579 B1	08-13-2002	Wang et al.	
	0041	US-6,445,245 B1	09-03-2002	Schultz et al.	
	0042	US-6,448,813 B2	09-10-2002	Garlepp et al.	
	0043	US-6,466,063 B2	10-15-2002	Chen	
	0044	US-6,588,984 B1	07-01-2003	Kent et al.	
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	0046	US-6,603,329 B1	08-05-2003	Wang et al.	
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	0048	US-6,642,741 B2	11-04-2003	Metz et al.	
A	0049	US 2002/0010853 A1	01-24-2002	Trimberger et al.	
	0050	US 2002/0060602 A1	05-23-2002	Ghia et al.	
	0051	US 2002/0101278 A1	08-01-2002	Schultz et al.	
	0052	US 2003/0062922 A1	04-03-2003	Douglass et al.	
	0053	US 2004/0008054 A1	01-15-2004	Lesea et al.	

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Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
he	0054	Altera, Apex 20K "Programmable Logic Device Family," Altera Corporation, Ver. 1.1, May 2001	/
	0055	Altera, Apex II "Programmable Logic Device Family," Altera Corporation, Ver. 1.1, May 2001	/
	0056	Bendak, M. et al. (1996). "CMOS VLSI Implementation of Gigabyte/second computer network links," Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407, IEEE International Symposium on Circuits and Systems pp.269-272.	/
	0057	Boni, A. et al. (2001). "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-um CMOS," IEEE Journal of Solid-State Circuits, 36(4):706-711.	/
	0058	Esch and Manley, Theory and Design of CMOS HSTL I/O Pads, The Hewlett Packard Journal, Aug, 1998	/
	0059	Xilinx, "Spartan-3 1.2V FPGA Family: Functional Description," Xilinx, DS099-2 (v1.2) July 11, 2003	/
	0060	Xilinx, "Virtex-II 1.5V Field Programmable Gate Arrays," Xilinx, DSO3102 (v1.5), Apr. 2, 2001	/
	0061	Xilinx, "Virtex-II Platform FPGAs: Detailed Description," Xilinx, DS031-2 (v3.1) October 14, 2003	/
he	0062	Xilinx, "Virtex-II Pro Platform FPGAs: Functional Description," Xilinx, DS083-2 (v2.9) October 14, 2003	/

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ME	0001	US-5,955,911	09-21-1999	Drost et al.	
ME	0002	US-6,489,837 B2	12-03-2002	Schultz et al.	

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